

Disruptive Photonics Technologies
for a New Generation of **Artificial
Intelligence** and **Data Center
Communications**

Dr. Suresh Venkatesan
POET Technologies

**1 Trillion Edge
Devices**
added in the
next 15 years

(Source: ARM)

**Explosion of
Data
generation**

5X Increase in the next 5
years

90% Generated by Machines

Shift from
General
Purpose to
**workload
specific
computing**

High Bandwidth , High Speed Connectivity
to move data between the Edge and the Cloud

Photonics 1.0

1980-2000 : Birth of the Internet

INTRODUCTION OF
Trans-oceanic Telecommunications
on Fiber Optic Cables



Photonics 2.0

2005-2025 : Web2.0 / Social Media / 3D Sensing

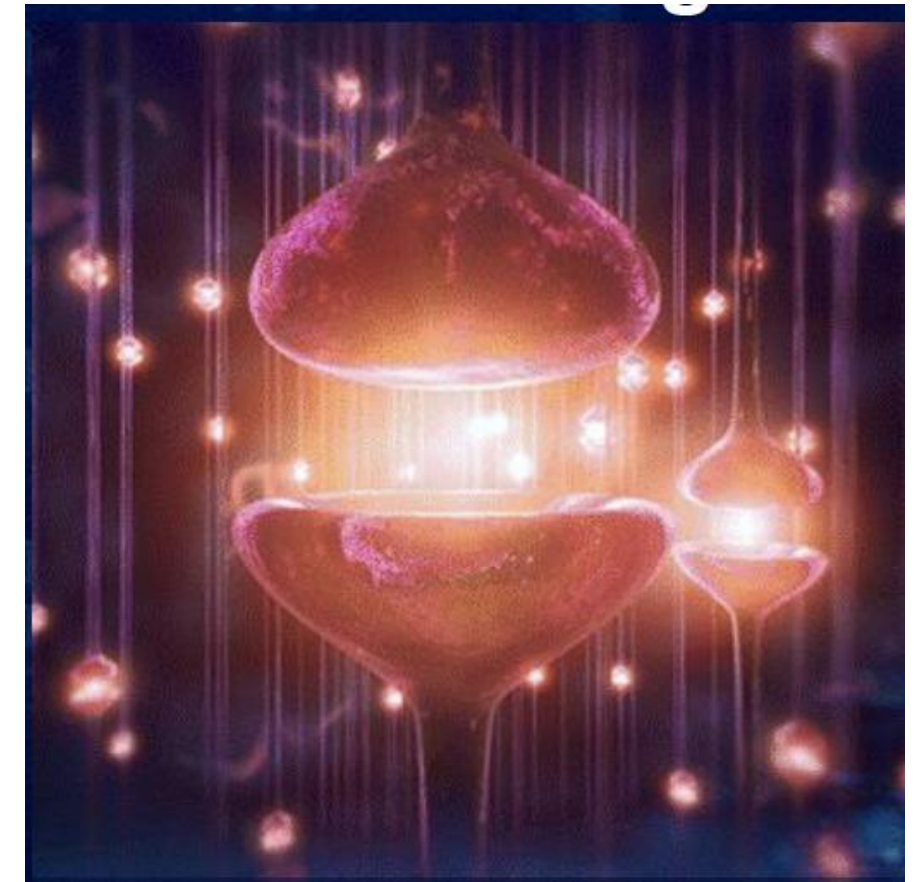
PROLIFERATION OF
Cloud Computing and
Growth of Internet



Photonics 3.0

2025+ : Entering the Future !!

GROWTH OF
Artificial Intelligence, 5G
and Edge Computing



The unique advantages of Optical Communications



High Throughput
> 1Tb/s channels

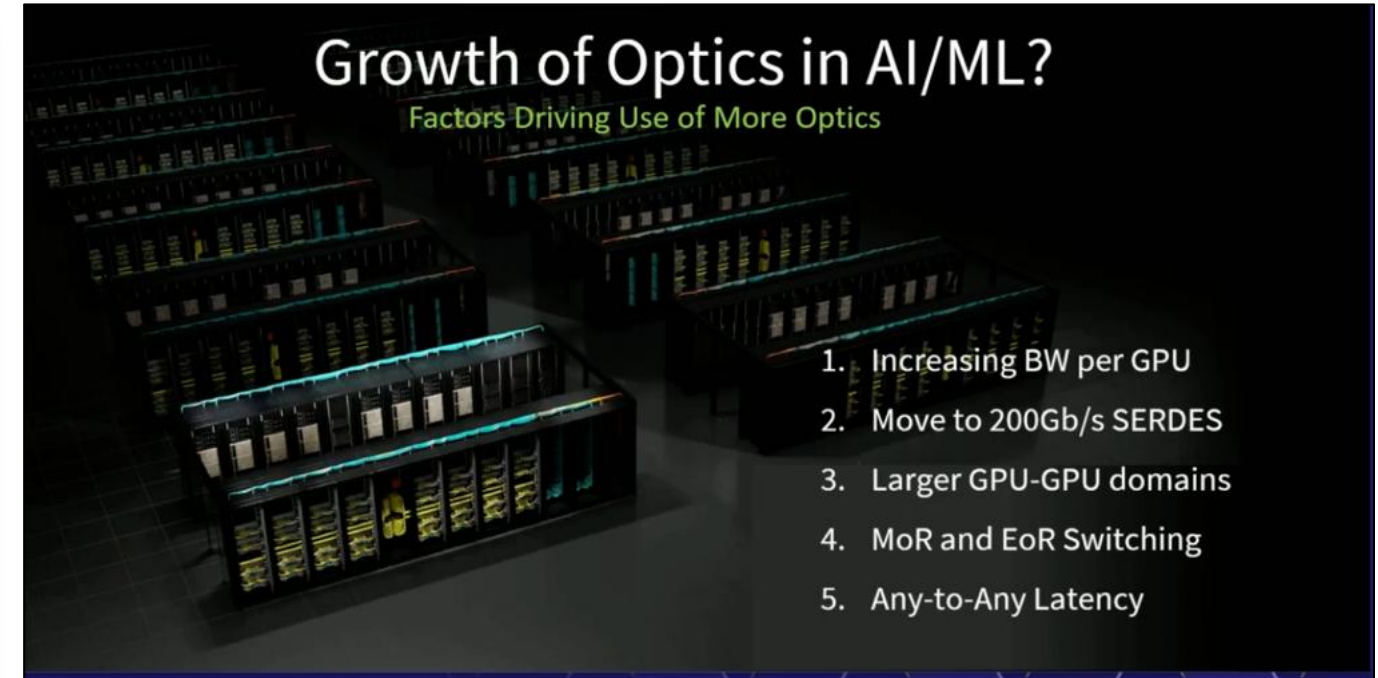


Energy Efficient
No Electrical Resistance



Low Latency
Transmit at the speed of light

AI Training places significant demands on latency and power



Growth of Optics in AI/ML?

Factors Driving Use of More Optics

1. Increasing BW per GPU
2. Move to 200Gb/s SERDES
3. Larger GPU-GPU domains
4. MoR and EoR Switching
5. Any-to-Any Latency

AI Workload

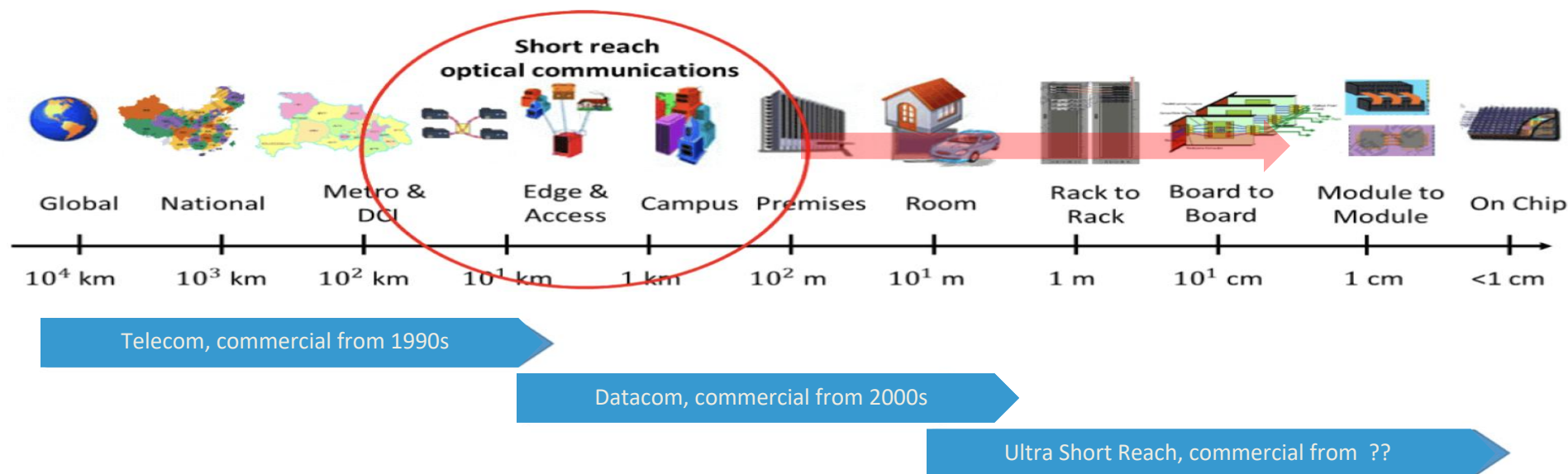
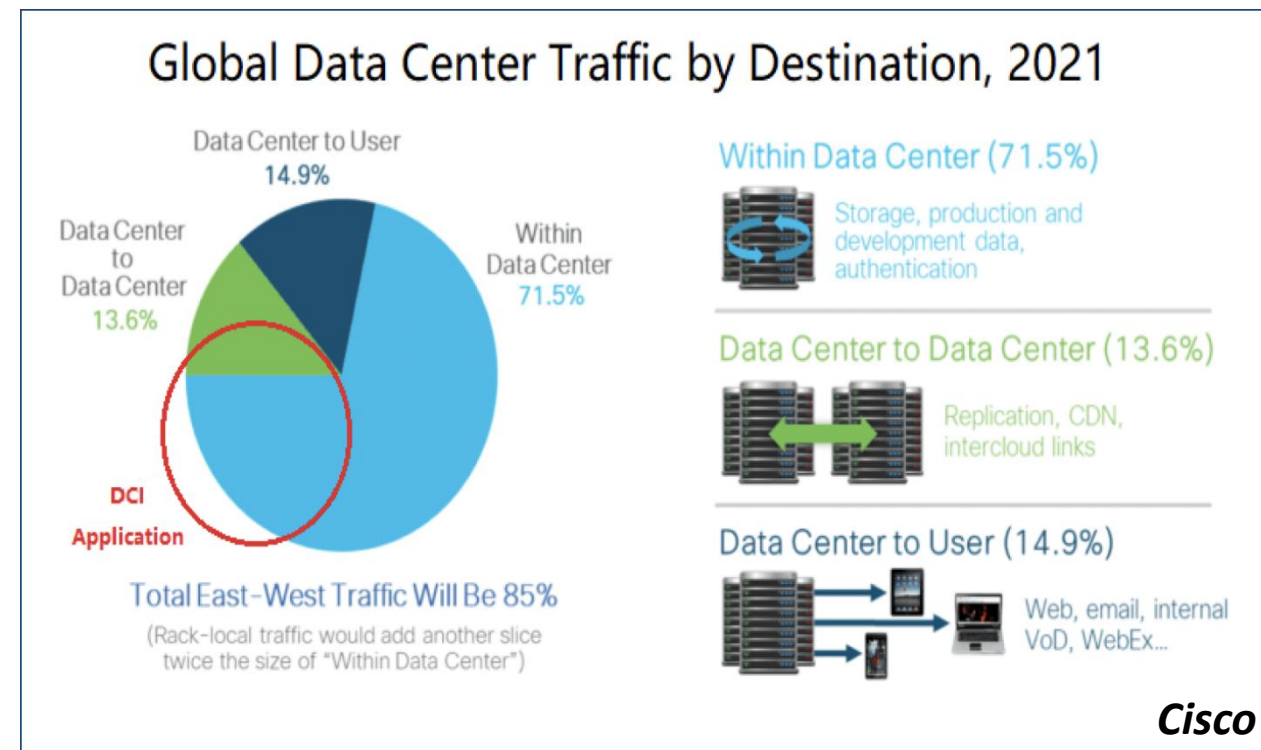
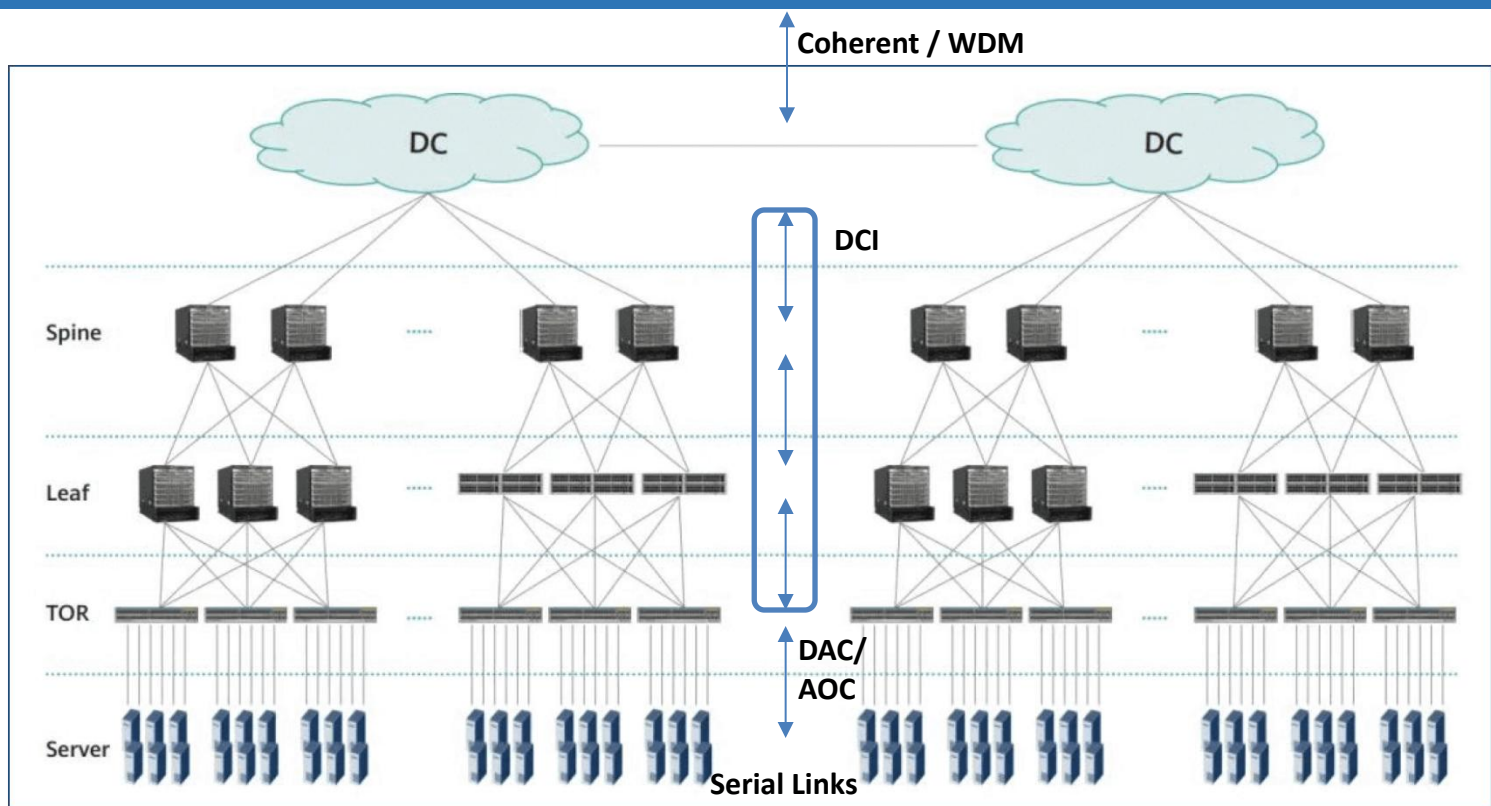
- Need to lower Power and reduce latency
- Disaggregation of GPU / Memory
- **Increase in the # of optical links for low latency communications between disaggregated servers**

Increasing demand for photonics solutions

Lightcounting: AI will add \$17B in optical transceiver sales over the next 5 years

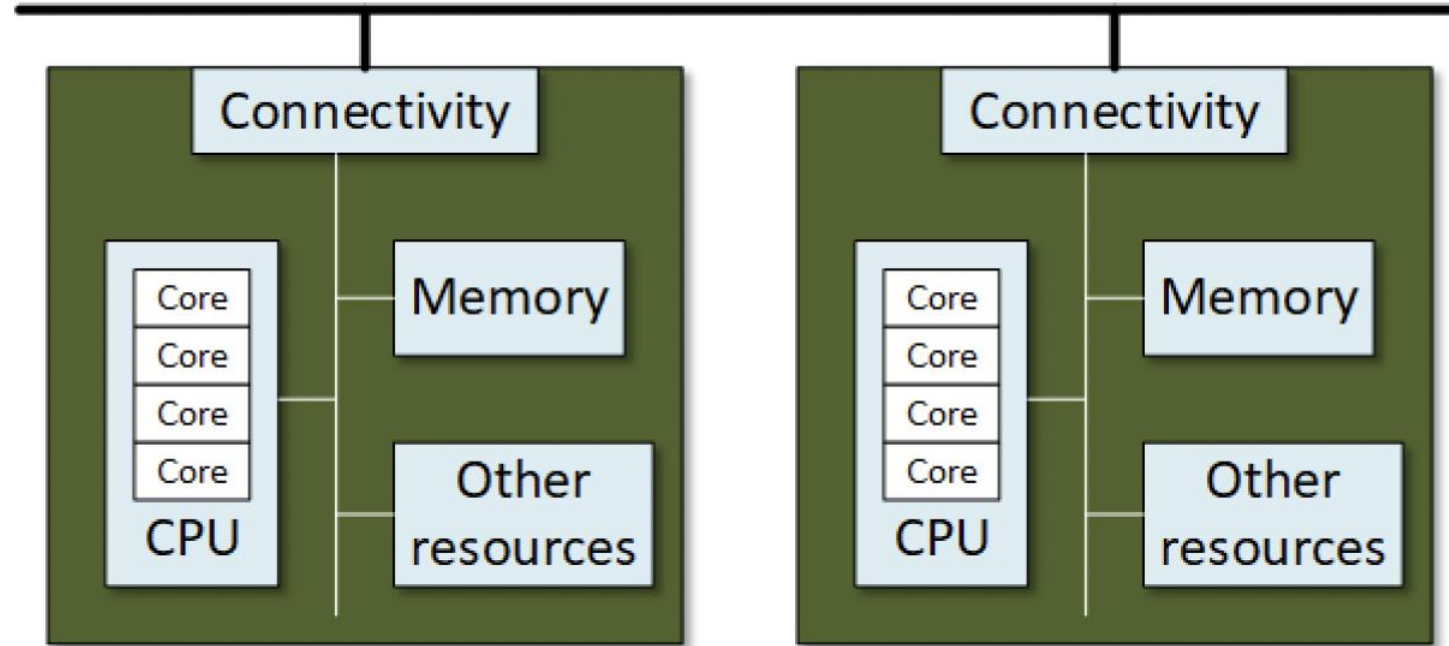
Dell ‘Oro: AI infrastructure spending to bring data center capex to >\$500B by 2027

Conventional Data Center Architectures

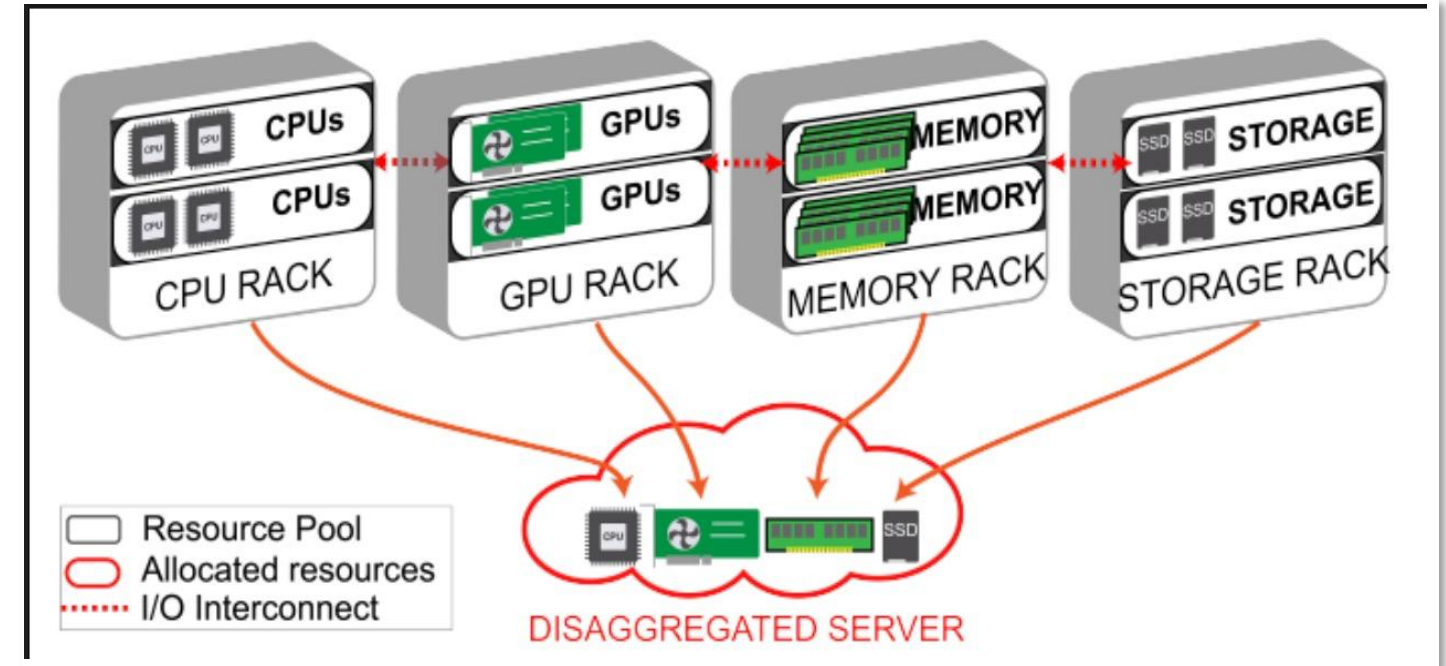


Architectures and Data Workloads increasingly supporting "short reach" communications

Conventional Architecture : A server blade is a “base” unit



Disaggregated Architecture : Composable resources



With the conventional processor-centric computing architecture and copper interconnects, the state-of-the-art chips based on 3nm technology are approaching their physical limitations, while the necessity for faster data transmission has surged.

Tradeoff between optimal utilization and the need for low latency.
Disaggregation is going to push the need for photonic connectivity.

The case for **INTEGRATION** in Photonics

Incumbent technologies are not scalable for applications needing 100's of millions and billions of units per year

Millions/Year

VECTOR

INCUMBENT TECHNOLOGIES*

COMPLETE PHOTONICS INTEGRATION

Unit Volume

X

✓

100s of Millions/Year

Size/Channel Count

X

✓

Cost

X

✓

Power Consumption

X

✓

Billions/Year

Photonics Integration Approaches

Production Costs	InP	Si Photonics (external laser)	Hybrid Integration	Heterogenous Integration on SOI	Epitaxial Growth on Silicon
III-V Substrate	✓	✓	✓	✓	
III-V Growth	✓	✓	✓	✓	✓
SOI substrate		✓		✓	
Silicon substrate			✓		✓
Assembly Costs	Full Active Alignment	Active Laser Coupling	Wafer scale passive bonding	III-V Chiplet Dicing / Bonding	
Testing	Die Level	Laser, Silicon PIC, Package	KGD, Wafer Level	Wafer Level	Wafer Level
Pros	Proven, reliable, great performance from laser, modulator, photodetector	Excellent passives performance; excellent yield allowing for complex levels of integration; can use known good die for light source	Excellent passive performance ; Low Loss and Non Birefringent ; Electrical and Optical Passive Capability ; Best of Breed	Combines III-V active functionality with silicon passive circuitry; integration of diverse epitaxial layers with common silicon waveguide	Lowest cost solution; complete active passive technology suite possible;
Cons	Cost / Scale	Strong reflections from high index contrast ($Dn \sim 2$); Laser needs external isolator; Complex receiver solutions	Separate processing of active and passive elements to result in best of breed component selection The most cost effective and deployable solution now	High thermal impedance of SOI substrate; strong reflections from high index contrast ($Dn \sim 2$); cost of laser epi and bonding; bond/laser yield affects entire package.	Material quality needs improvement; Not all materials are conducive to defect free epitaxial growth on Silicon

Silicon Photonics OR Silicon for Photonics ?

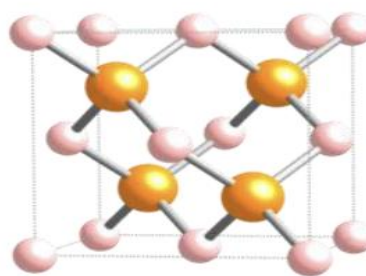
Conventional Silicon Photonics has been disappointingly and agonizingly slow to penetrate DCI (Pluggables)

- Only a transmit solution (for most part)
- Lossy Modulator – marginal performance at 100G/lane
- Presence PRIMARILY in parallel optics – not in WDM
- Yield / Cost
- Power Parity with EML solutions
- “Missing in action” so far @ 200G/lane

Silicon photonics is moving towards more materials integration



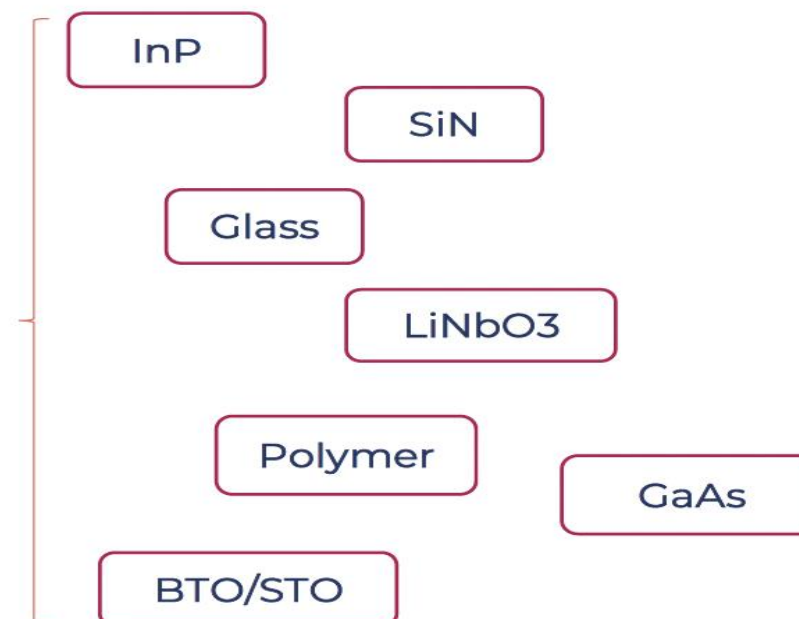
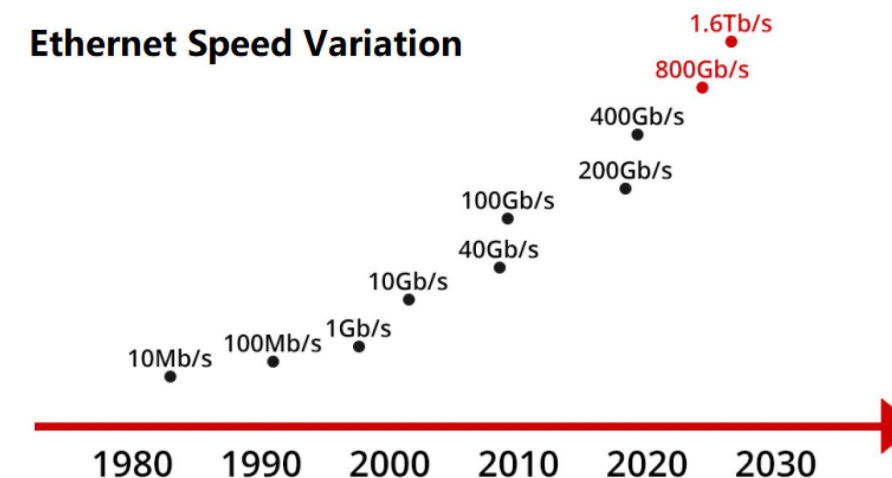
SOI



InP



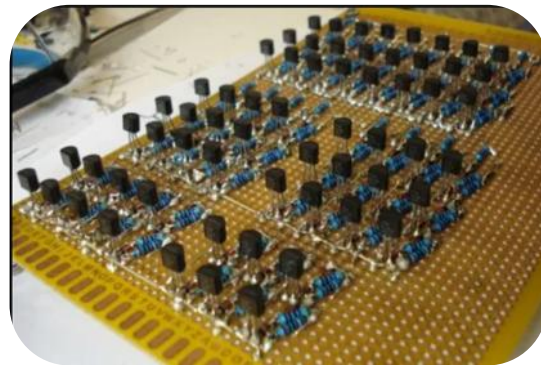
More materials integration in the future, using CMOS platform.



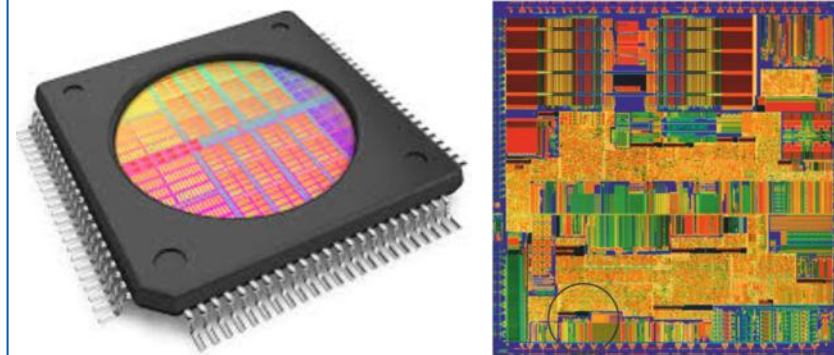
POET does for Photonics what Integrated circuits did for electronics

Semiconductor Electronics

Discrete Components



Integrated Circuit



Moore's Law

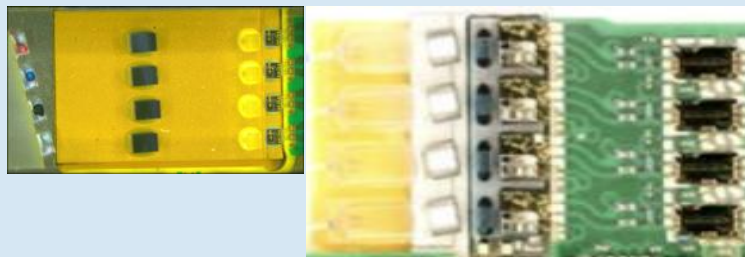
- Smaller, Faster, Cheaper, Volume
- Transformed the industry - pervasive presence of semiconductors
- Trillion dollar industry - grown over three decades of investment

Photonics

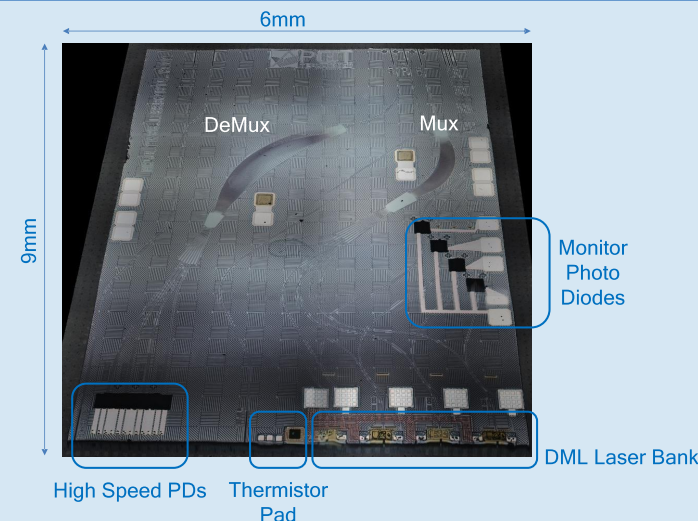
Discrete Transceiver Assembly

100G

400G



- ~50 individual components and sub-systems
- High labor and equipment cost - cannot scale



World's smallest optical engines for pluggable applications

POET Optical Interposer Platform

- Automated integration of components on a single chip
- Economies of scale comparable to semiconductors
- Transformational technology for Photonics

Wafer scale assembly. Passive alignments. Eliminate wire bonds.

Wafer Level Packaging & Testing

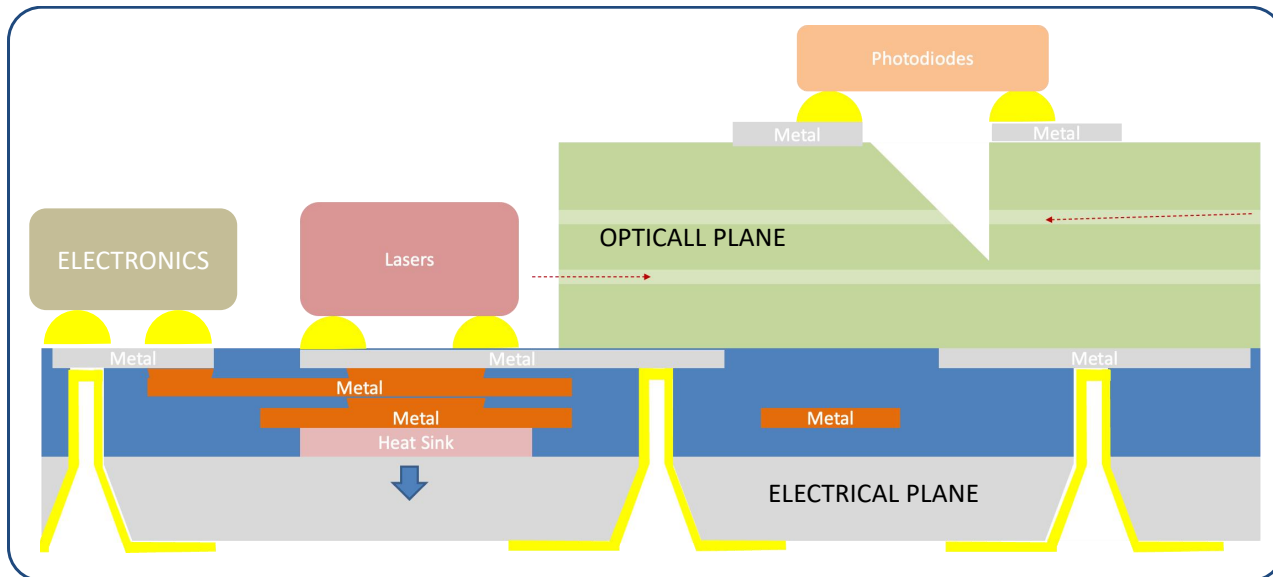
- Use automated pick-place equipment to enable high speed and low-cost manufacturing
- Reduce industry assembly costs from as much as 70% to less than 20%
- Passive Laser placement with high coupling efficiency
- Significant departure from component level testing which much of the industry does

Passive Alignments

- Eliminate active alignments of Lasers to lens, isolators and optical MUX
- Significant reduction of CapEx and OpEx by eliminating active alignments
- Enables high volume production without large investments

Eliminate Wire bonds

- Achieve semiconductor type placement of Optical Engines on PCB with solder bumps (no more wire-bonds)
- Improve RF performance with high-speed trace instead of gold wire bonds
- Reduce cost

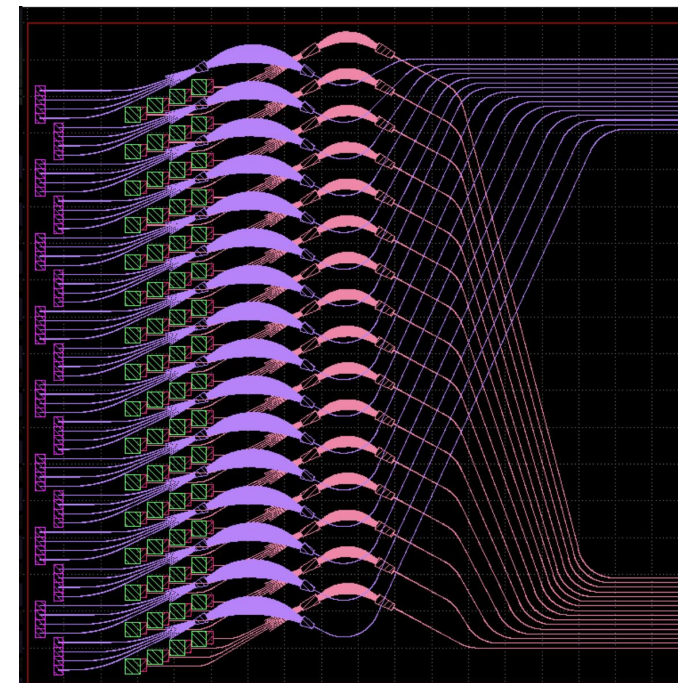


INTERPOSER KEY FEATURES

- Hybrid integration of known good die
- Works with DML, EML, SiPh, TFLN
- Built-in low loss micro mirrors
- CMOS compatible low loss waveguides
- Monolithically integrated AWG MUX and DMUX
- Mode matching SSC

- Two layers of low loss optical interconnects
- Multiple electrical redistribution layers with low RF insertion loss
- High throughput visually assisted passive “pick and place” assembly of electronics and photonics ICs and components
- In plane and Out of plane Optical Interfaces

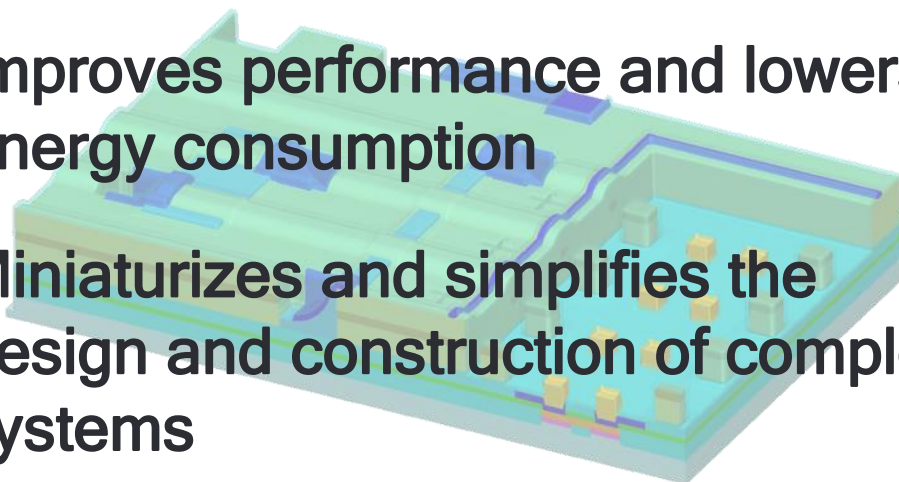
Optical Interposer Platform enabling >700GBps per mm



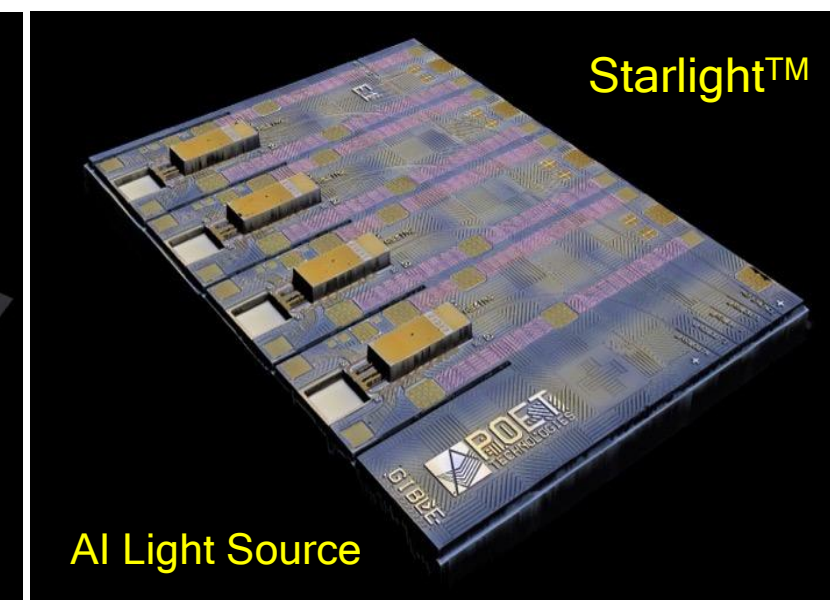
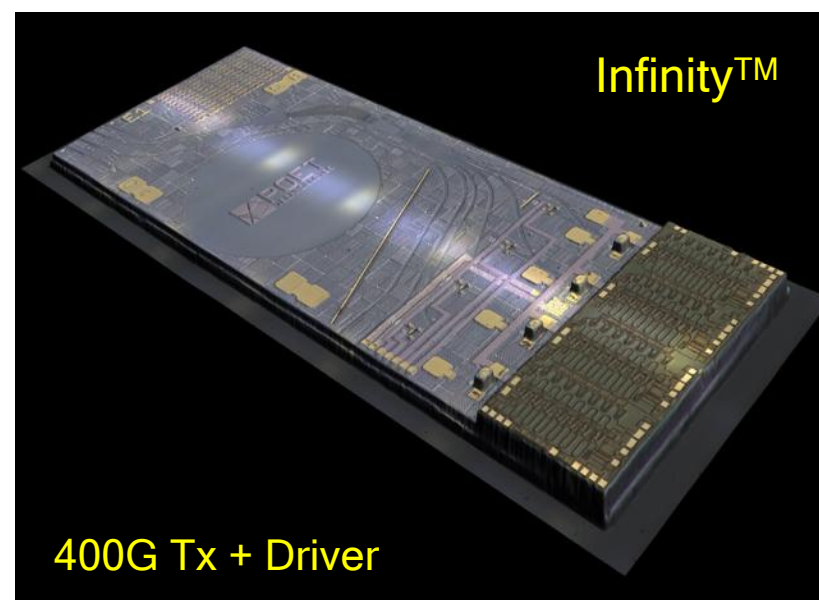
16 lanes of communication using 3D assembly techniques and stacked non-interacting waveguides in a 18mm “shoreline”

A proprietary technology platform for integrating photonic solutions

- Drives down the cost of component integration and packaging
- Improves performance and lowers energy consumption
- Miniaturizes and simplifies the design and construction of complex systems
- Provides unparalleled scale through wafer level processing



POET's Optical Interposer-based Optical Engines and Light Sources



Scalable



Inexpensive



Low-power



Simple

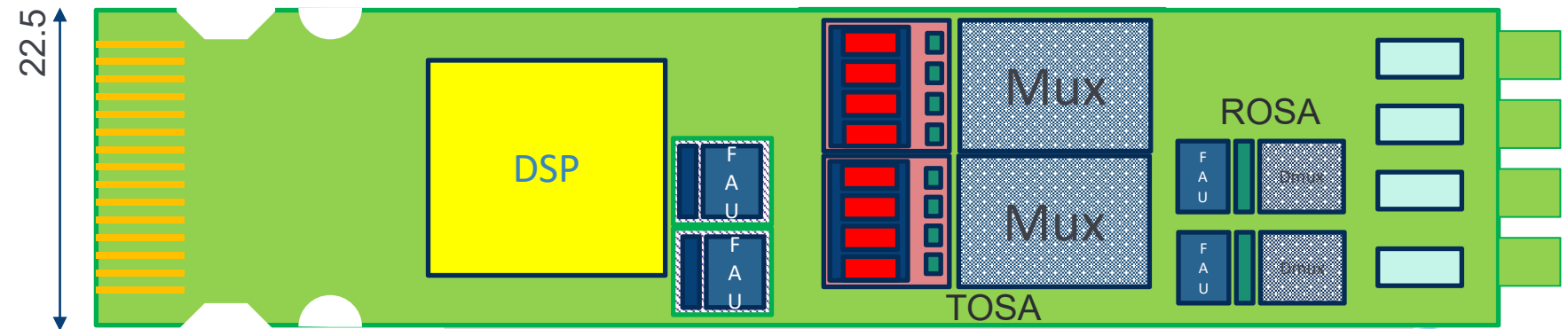
Simplified Design, Improved Energy and Lower Cost

Data Communications Challenges

- Serial data communication channels have not been able to keep up with the pace of bandwidth growth.
- Number of communications lanes increase as data rate increases!

Data Rate	Number of lanes
10G	1
40G	4
100G	1/4
200G	4
400G	4
800G	8
1.6T	8
3.2T	16

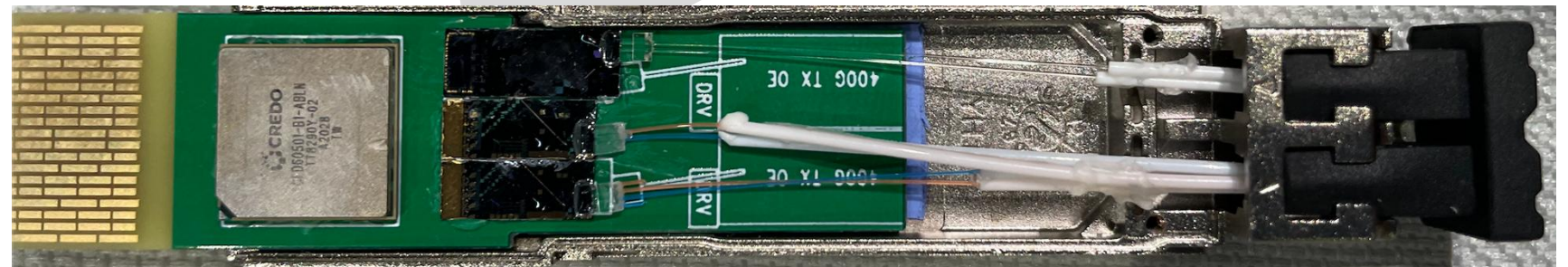
Conventional Discrete Assembly



- ~50 individual pieces; multiple active alignments
- Unsustainable for 8 channels ; Impossible for 16

**POET :
75% smaller**

POET's Hybrid Integration

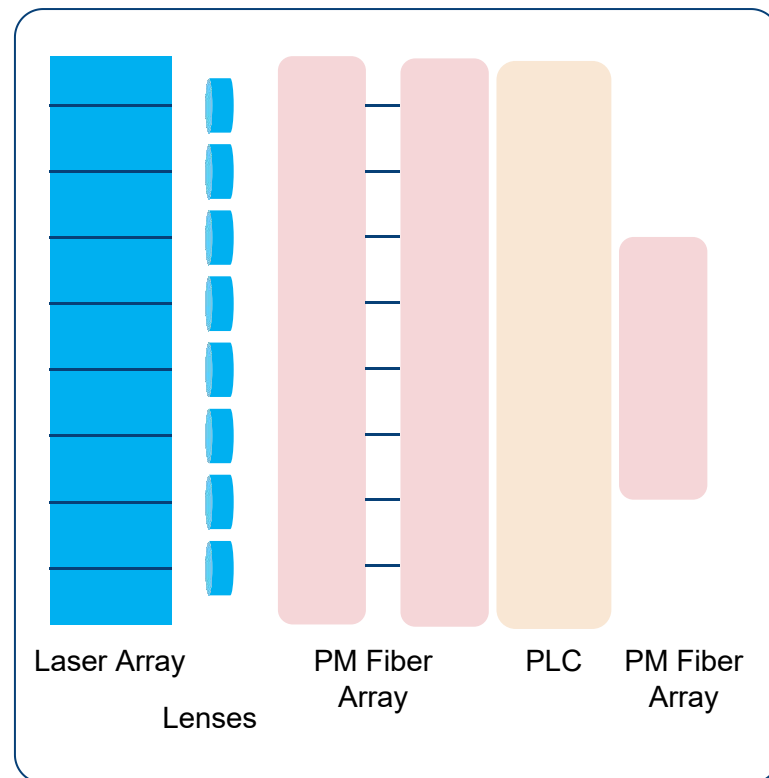


- Integrated Tx and Rx optical engines with no active alignment
- Readily scalable to 16 channel implementations

How POET solutions **lower the cost** of the External Light Source

Interposer approach enables unparalleled performance and cost benefits

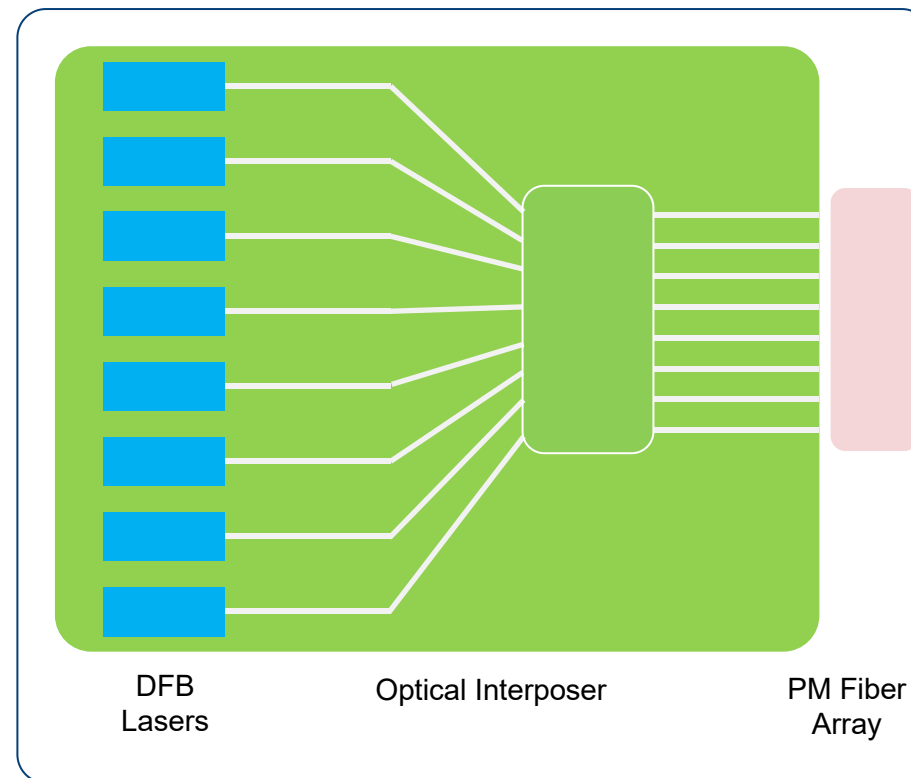
Incumbent Solutions



- Laser Arrays
- Active alignment
- Separate PLC (if required) for multiplexing
- PM fiber attach – expensive

-75%

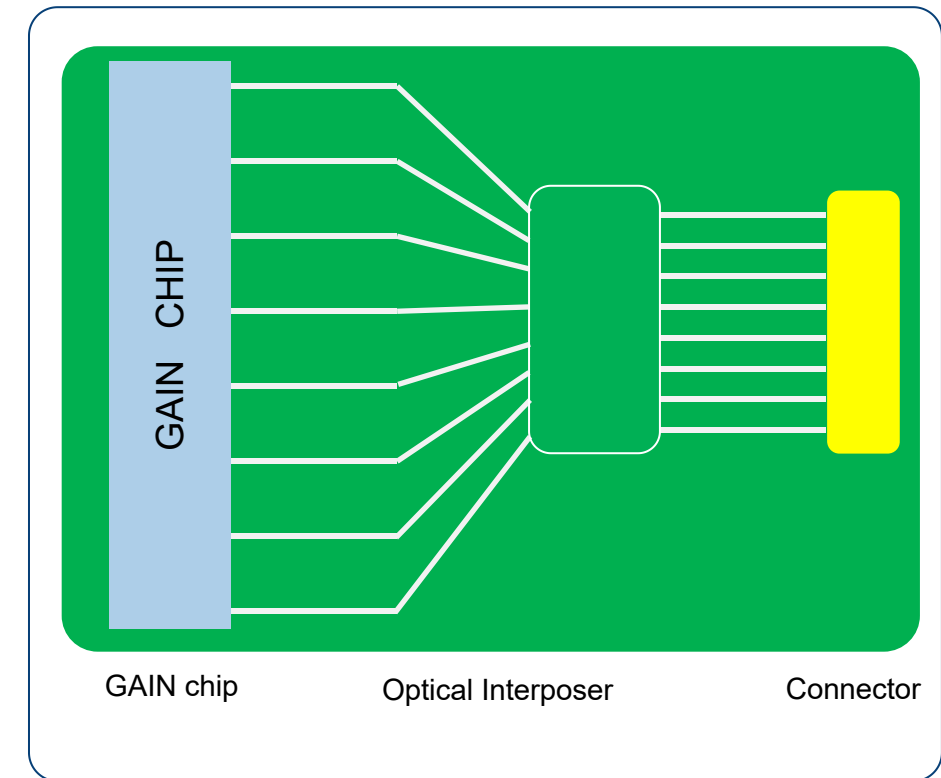
Interposer Solutions



- Passively placed individual lasers at wafer scale
- All PLC functionality incorporated into interposer
- Single chip solution
- PM fiber attach – remains on host side

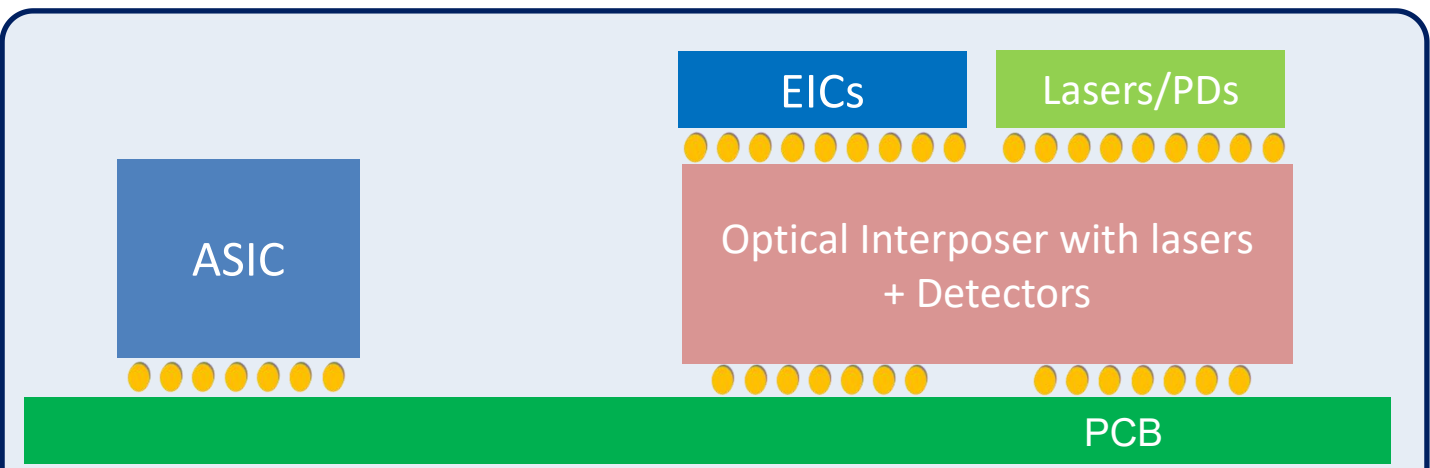
-85%

Hybrid Laser Solutions

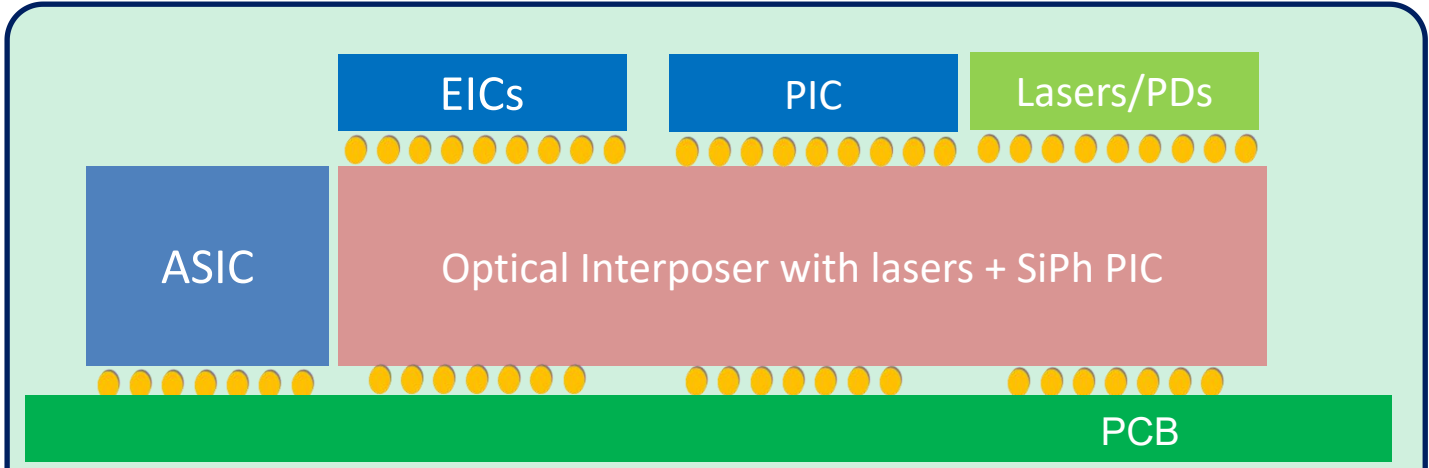


- Passively placed gain chip at wafer scale
- All PLC functionality incorporated into interposer
- Athermal lasing – no cooling required even at 200GHz spacings
- PM fiber replaced by connectors on host side.

Interposers enable Flexible Architectures for multiple applications

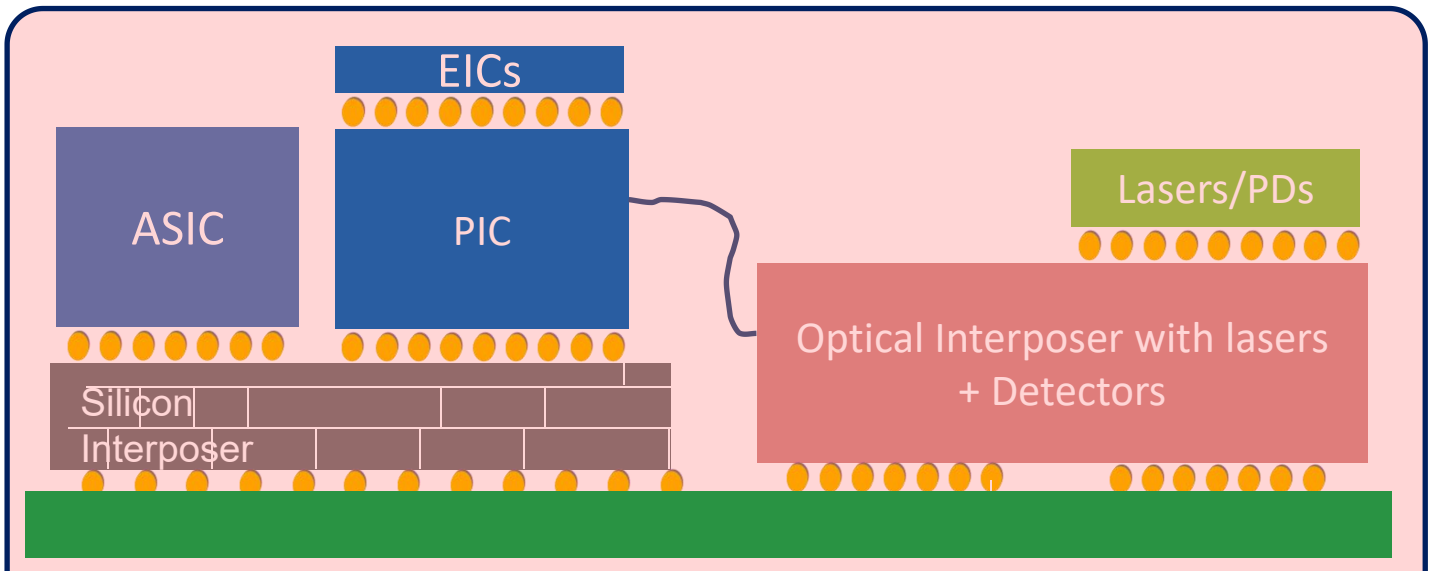
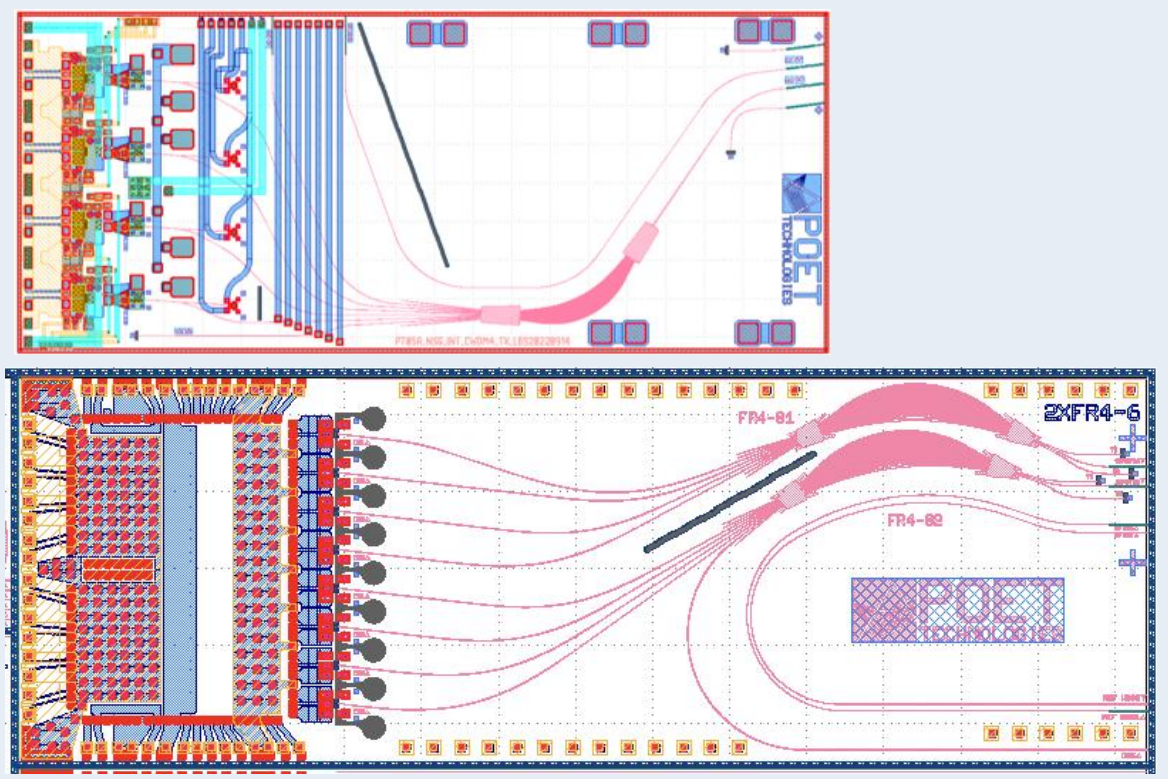


Modulated Laser solutions using the Optical Interposer



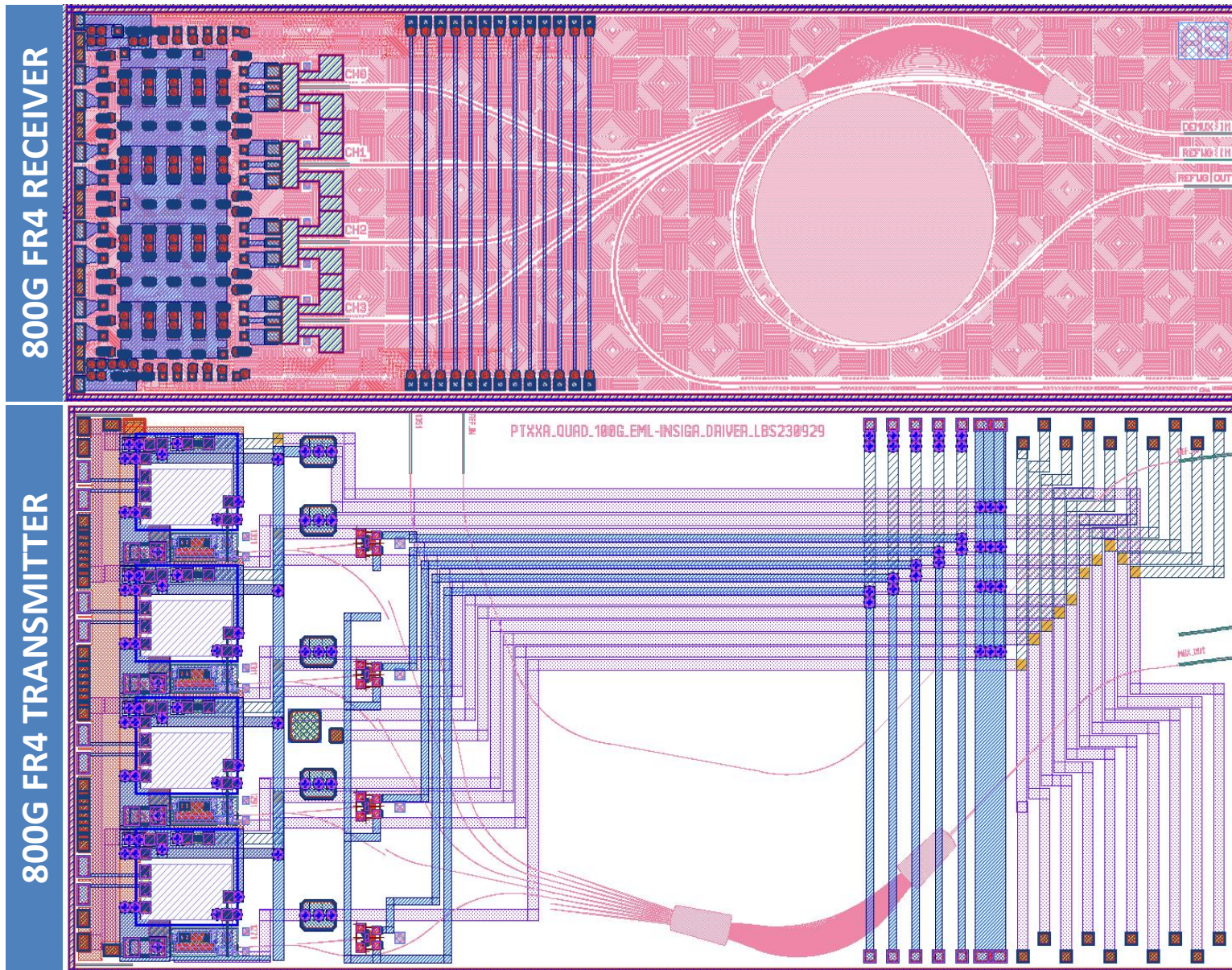
Integrated Laser/PIC solution using the Optical Interposer

800G Products with Integrated Hybrid Electronics



External Laser solutions using the Optical Interposer

Solutions scalable to 1.6T and 3.2T architectures with 200G/lane components



Highly Scalable Solutions enabling 3.2Tbps PLUGGABLE OPTICS

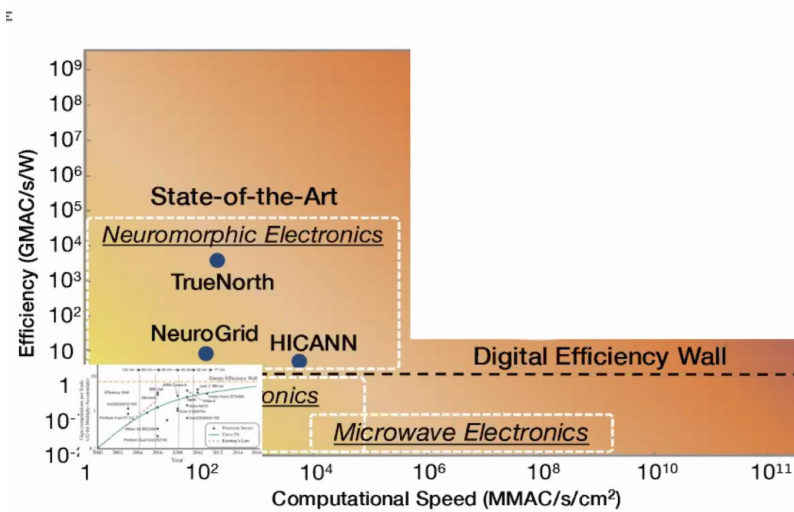
- Support for Externally Modulated Lasers and Drivers
- Support for Backside Illuminated High Speed Photodiodes
- >75GHz RF Transmission Lines
- Through Silicon Vias
- Onboard support for SMD components for “point of use” decoupling
- Integrated MIM capacitors for high frequency filtering

SAMPLING SOLUTIONS IN 1H 2024 !!

Linear Algebra (encoding data as continuous signals) → Perfectly suited for Analog compute

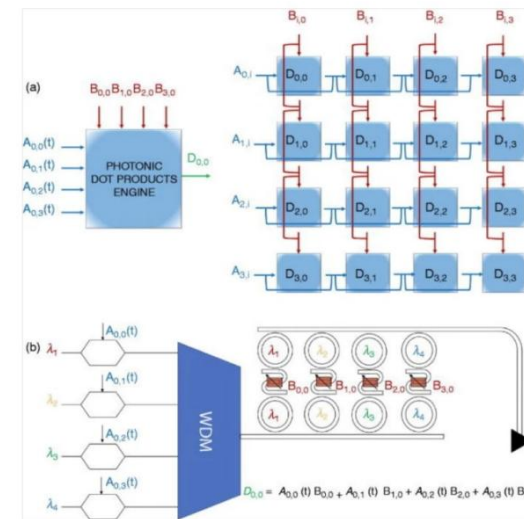
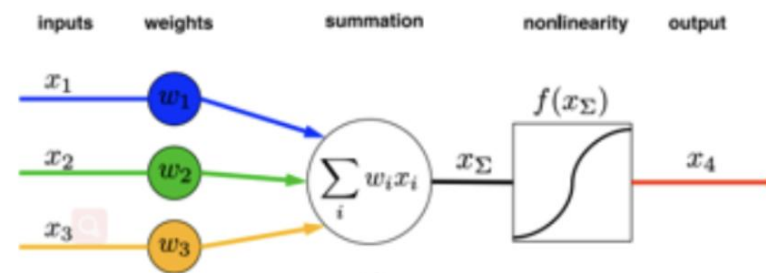
- Perfectly suited for artificial neural networks, Machine Learning and AI
- Manipulates matrices
- With appropriate modulating devices, it is possible to encode data using light beams and subsequently manipulate the data

The Rise of Neuromorphic Computing



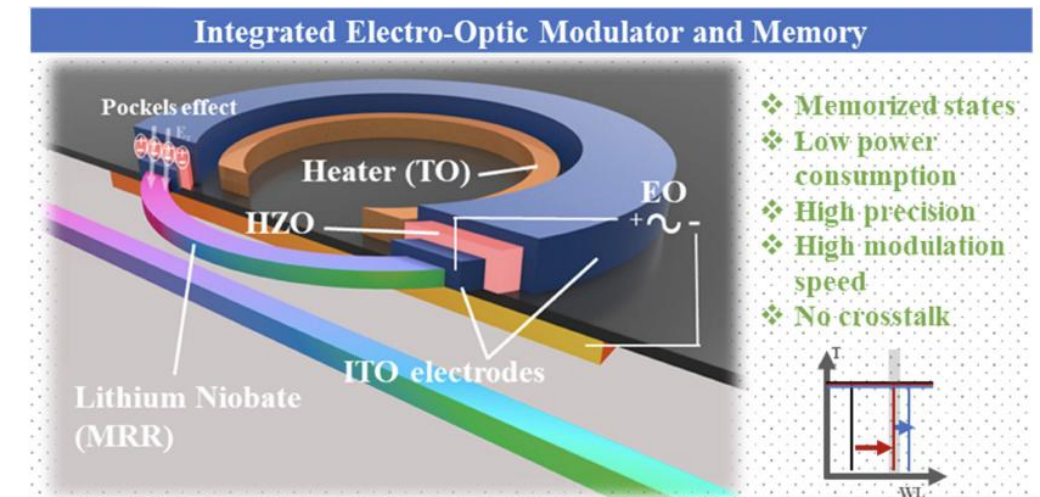
P. Prucnal and V. J. Sorger groups, ACP 2018
Nikos Pleros, 2019

- Neuromorphic computing will breach the energy efficiency wall
- Neuromorphic Photonics: **A natural analog platform**



First Demonstration of HZO-LNOI Integrated Ferroelectric Electro-Optic Modulator and Memory to Enable Reconfigurable Photonic Systems

Zefeng Xu^{1,2,6†}, Chun-Kuei Chen^{1,6†}, Hong-Lin Lin^{1†}, Yuan Gao¹, Wei Ke³, Baochang Xu^{1,6}, Pavel Dmitriev⁴, Carlan Arbiz⁵, Evgeny Zamburg^{1,6}, Steven Touzard⁴, Xinlun Cai³, James Lee⁵, Suresh Venkatesan⁵, Aaron Danner¹, Aaron Voon-Yew Thean^{1,2,6*}



AI based on deep learning is developing fast. Hardware which can speed up that development still more is the key



- Increasing electrical and optical data rates (electrical – 28Gbps to 224Gbps ; optical – 25G/λ to 200G/λ)



- Increasing levels of integration in the module – wavelength division and spatial division multiplexing. Higher bandwidth density per mm (or mm²)



- Increased performance/Lower Power.



- High Volume ; Low Cost Manufacturing
- Fast product transitions
- Time to market



- Disaggregation and new architectures
- Photonics must approach serial copper links for pricing and power

Photonics Platform Requirements

- Integration is essential (co packaging of electronic and photonic die on a common substrate)
- Silicon “for” Photonics and not necessarily Silicon Photonics
- Best of Breed component integration
- Efficient Optical Passives
- Flexibility to incorporate discrete components through wafer scale high volume assembly
- Low Loss, Low Cost, High Scale, Flexible
- Wafer Scale with high degree of automation
- Must support high RF bandwidth requirements
- Must support the diverse requirements of : Electrical, Mechanical, Optical and Thermal

